In the claims

Please AMEND claim 1, CANCEL claims 10 and 19-59 without prejudice, and ADD new claims 60-70 so that the claims to read as follows:

1. (Currently Amended) A semiconductor die comprising:

a substrate device level comprising substrate transistors, the substrate transistors having a substrate pitch, some portion of each of the substrate transistors formed in a monocrystalline substrate; ~~and~~

a first above-substrate device level formed above the substrate device level, the first above-substrate device level comprising first above-substrate devices having a first above-substrate pitch, wherein the first above-substrate pitch is smaller than the substrate pitch; and

a second above-substrate device level formed over the first above-substrate device level, the second above-substrate device level having a second above-substrate pitch, wherein the second above-substrate pitch is smaller than the substrate pitch.

2. (Previously presented) The semiconductor die of claim 1 wherein the first above-substrate devices of the first above-substrate device level comprise~~s~~ a first plurality of memory cells, the memory cells at the first above-substrate pitch.

3. (Previously presented) The semiconductor die of claim 2 wherein the substrate transistors of the substrate device level comprise~~s~~ driver circuitry.

4. (Previously presented) The semiconductor die of claim 3 wherein the first above-substrate device level comprises:

a first area, said first area comprising portions of the first plurality of memory cells, the memory cells having the first above-substrate pitch; and

a second area, said second area having a fan-out pitch, wherein said fan-out pitch is larger than the first above-substrate pitch.

5. (Original) The semiconductor die of claim 4 wherein the first area comprises a plurality of substantially parallel, substantially coplanar rails.

6. (Original) The semiconductor die of claim 5 wherein photolithography processes are optimized to minimize the first above-substrate pitch of the plurality of rails in the first area.

7. (Original) The semiconductor die of claim 6 wherein the plurality of rails is patterned using off-axis illumination.

8. (Original) The semiconductor die of claim 7 wherein the plurality of rails is patterned using a dipole illumination aperture.

9. (Canceled)

10. (Canceled)

11. (Original) The semiconductor die of claim 5 wherein the rails comprise a first plurality of memory lines

electrically connected to a first plurality of vertical interconnects at a first end and a second plurality of memory lines electrically connected to a second plurality of vertical interconnects at a second end opposite the first end, the first and second pluralities interleaved.

12.(Original) The semiconductor die of claim 2 wherein the plurality of memory cells form part of a monolithic three dimensional memory array.

13.(Original) The semiconductor die of claim 12 wherein the memory array comprises segmented bit lines and global bit lines, wherein two segmented bit lines share a vertical connection to an associated global bit line.

14.(Canceled)

15.(Original) The semiconductor die of claim 2 wherein the memory cells are passive element memory cells.

16.(Previously presented) The semiconductor die of claim 15 wherein the memory cells are antifuse-diode cells.

17.(Original) The semiconductor die of claim 2 wherein the memory cells are thin film transistors having a charge-storage dielectric.

18.(Original) The semiconductor die of claim 17 wherein the memory cells are arranged in series-connected NAND strings.

19. (Canceled)

20. (Canceled)

21.(Canceled)

22.(Canceled)

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53.(Canceled)

54.(Canceled)

55.(Canceled)

56.(Canceled)

57.(Canceled)

58.(Canceled)

59.(Canceled)

60.(New) A semiconductor die comprising:

a substrate device level comprising substrate transistors, the substrate transistors having a substrate pitch, some portion of each of the substrate transistors formed in a monocrystalline substrate, wherein the substrate transistors of the substrate device level comprise driver circuitry; and

a first above-substrate device level formed above the substrate device level, the first above-substrate device level comprising first above-substrate devices having a first above-substrate pitch, wherein the first above-substrate pitch is smaller than the substrate pitch, wherein the first above-substrate device level comprises:

a first plurality of memory cells, the memory cells at the first above-substrate pitch;

a first area, said first area comprising:

portions of the first plurality of memory cells, the memory cells having the first above-substrate pitch; and

a plurality of substantially parallel, substantially coplanar rails, wherein the rails comprise a first plurality of memory lines electrically connected to a first plurality of vertical interconnects at a first end and a second plurality of memory lines electrically connected to a second plurality of vertical interconnects at a second end opposite the first end, the first and second pluralities interleaved; and

a second area, said second area having a fan-out pitch, wherein said fan-out pitch is larger than the first above-substrate pitch.

61.(New) The semiconductor die of claim 60 wherein photolithography processes are optimized to minimize the first above-substrate pitch of the plurality of rails in the first area.

62.(New) The semiconductor die of claim 61 wherein the plurality of rails is patterned using off-axis illumination.

63.(New) The semiconductor die of claim 62 wherein the plurality of rails is patterned using a dipole illumination aperture.

64.(New) The semiconductor die of claim 60 further comprising a second above-substrate device level formed over the first above-substrate device level, the second above-substrate

device level having a second above-substrate pitch, wherein the second above-substrate pitch is smaller than the substrate pitch.

65.(New) The semiconductor die of claim 60 wherein the plurality of memory cells form part of a monolithic three dimensional memory array.

66.(New) The semiconductor die of claim 65 wherein the memory array comprises segmented bit lines and global bit lines, wherein two segmented bit lines share a vertical connection to an associated global bit line.

67.(New) The semiconductor die of claim 60 wherein the memory cells are passive element memory cells.

68.(New) The semiconductor die of claim 67 wherein the memory cells are antifuse-diode cells.

69.(New) The semiconductor die of claim 60 wherein the memory cells are thin film transistors having a charge-storage dielectric.

70.(New) The semiconductor die of claim 69 wherein the memory cells are arranged in series-connected NAND strings.